IN THE SPECIFICATION:

Please amend the specification as follows:

Please replace the paragraph on page 9, lines 11-20 with the following paragraph:

-- Figure 6 is a flowchart of a method 60 for generating a model for a circuit in accordance with one embodiment of the present invention. Method 60 begins at a block 62, in which a netlist model is generated for the circuit. The netlist model is a logic gate level description of the circuit that is used by ATPG to generate test patterns that are applied to the actual circuit to test for defects (e.g. at block 68). In a block ~~62~~ 64, a virtual delay element is provided to the netlist model. The virtual delay element is coupled to an asynchronous circuit element (or a combination of circuit elements that demonstrate asynchronous behavior) and provided along paths where race resolution is required. By controlling a virtual clock that enables the virtual delay element (e.g. at block 66), either the user or ATPG may impose an order in which signals arrive at any component in the circuit. --